Application No. 10/510,299
Discussion Amendment

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Previously Presented) A method, comprising:

synchronising start of cell times in input/output circuits with cell transmission periods in a cross-connection circuit,

transferring cells between said input/output circuits by said cross-connection circuit in cell transfer periods,

changing configurations of said cross-connection circuit between cell transfer periods in cross-connection configuration periods,

sending cells from a sending input/output circuit of said input/output circuits at start of cell times,

receiving said sent cells in said cross-connection circuit,

oscillating between a loopback configuration and a no-transmission configuration,

transferring the received cells back to said sending input/output circuit in said loopback configuration and not transferring the received cells back to said sending input/output circuit in said no-transmission configuration,

receiving back transferred cells in said sending input/output circuit during said loopback configuration,

checking said cells transferred back during said loopback configuration in said sending input/output circuit for a transmission error, and

shifting an offset of said start cell times in case a transmission error occurred, until transferring back at least one cell is wholly carried out within a cell transfer period.

2. (Previously Presented) A method according to claim 1, wherein the shifting includes shifting said offset of start of cell times in said sending input/output circuit,

respectively, to align the time sent cells from said sending input/output circuit are received in said cross-connection circuit.

3. (Previously Presented) A method according to claim 1, including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

4. (Previously Presented) A method according to claim 1, including calculating start of cell times based on a start of cell signal and said offset of said start of cell times, serializing said cells, and sending said serialized cells together with said start of cell signal at said start of cell times.

5. (Previously Presented) A method according to claim 1, including receiving transferred back cells, de-serializing said cells and checking each cell for transmission errors.

6. (Previously Presented) A method according to claim 1, including receiving transferred back cells, de-serializing said cells and evaluating a bit error indicator.

7. (Previously Presented) A method according to claim 3, wherein the shifting includes shifting said offset of start of cell times using an offset counter and changing said offset counter by an amount of clock cycles of said central clock signal.

8. (Previously Presented) A method according to claim 1, wherein the shifting includes shifting said offset of said start of cell times to a maximum without generating transmission errors, and shifting said offset of said start of cell times to a minimum without generating transmission errors.

9. (Previously Presented) A method according to claim 8, wherein the shifting includes setting said offset of said start of cell times in between said maximum and said minimum.

10. (Currently Amended) A packet switch comprising:

a plurality of port controllers each with a cell input port and a cell output port, and

cross-connection means including cell input ports and cell output ports connected to said cell output ports and cell input ports of said port controllers, respectively,

wherein a sending port controller of said port controllers comprises:

a start of cell signal generator for generating start of cell ~~signals,~~ signals;

an error detection means for detecting corrupt received cells; and

an offset controller for shifting a start of cell time ~~based on said~~ with respect to the start of cell ~~signal, and~~ signal based on whether any corrupt cells are detected;

~~an error detection means for detecting corrupt received cells,~~

wherein said cross-connection means comprises:

a configuration controller for controlling an oscillation of transfer periods between a loopback configuration, in which received cells are transferred back to a respective sending port controller, and a no-transmission configuration of said cross-connection means, ~~and~~ wherein the respective offset controller of the respective sending port controller is configured to ~~adjust~~ shift the start of cell time ~~based on detected corrupt cells received during the loopback configuration.~~ at least until an uncorrupted transferred back cell is received by the respective port controller during a transfer period.

11. (Previously Presented) A packet switch according to claim 10, further comprising a central clock generator for providing a central clock signal, wherein said start of cell signal generator, said offset controller, and said configuration controller each comprise an input port for said central clock signal.

12. (Previously Presented) A packet switch according to claim 10, wherein said sending port controller comprises a serializer and a de-serialize for serializing cells to be sent and de-serializing received cells.

13. (Previously Presented) A packet switch according to claim 10, wherein said cross-connection means comprise a $N \times N$ crossbar matrix, selectively connecting N cell input ports with N cell output ports.

14. (Currently Amended) A packet switch according to claim 13, wherein said loopback configuration is realized ~~realised~~ by a unit matrix and a no-transmission configuration is realised by a null matrix.

15. (Previously Presented) A packet switch according to claim 10, wherein said error detection means is a bit error indicator.

16. (Previously Presented) A method, comprising:

synchronizing start of cell times, in a packet switched network, for plural port controllers during a set up to allow configuration changes in a cross-connection circuit without disturbing cell transfers;

transferring cells between said port controllers by said cross-connection circuit in cell transfer periods;

changing configurations of said cross-connection circuit between cell transfer periods in cross-connection configuration periods;

sending cells from a sending port controller of said port controllers at start of cell times;

receiving said sent cells in said cross-connection circuit;

oscillating between a loopback configuration and a no-transmission configuration;

transferring the received cells back to said sending port controller in said loopback configuration and not transferring the received cells back to said sending port controller in said no-transmission configuration;

receiving back transferred cells in said sending port controller during said loopback configuration;

checking said cells transferred back in said sending port controller for a transmission error; and

shifting an offset of said start cell times in case a transmission error occurred, until transferring back at least one cell is wholly carried out within a cell transfer period.

17. (Canceled)

18. (Previously Presented) A method according to claim 16, wherein the shifting includes shifting said offset of start of cell times in said sending port controller, respectively, to align the time sent cells from said sending input/output circuit are received in said cross-connection circuit.

19. (Previously Presented) A method according to claim 16, including controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

20.-21. (Canceled)

22. (Currently Amended) A system, comprising:

a plurality of port controllers each having a cell input port configured to receive cells and a cell output port configured to transmit cells at start of cell times; and

a cross connection matrix coupled to the cell input ports and the cell output ports of the plurality of port controllers, the cross connection matrix having a configuration controller configured to control an oscillation of cell transfer periods during a setup of the system between

a loopback configuration, in which cells transmitted by a respective port controller are transferred back to the respective port controller, and a no transmission configuration, wherein ~~a sending port controller of~~ the plurality of port controllers comprises:

a start of cell signal generator configured to generate ~~a~~ start of cell ~~signals;~~ signals;

an error detector configured to detect errors in cells ~~received~~ transferred back to the respective port controller during the loopback configuration; and

an offset controller configured to shift a start of cell time for the respective port controller based on a start of cell signal and detected errors in ~~the~~ transferred back cells ~~received during the loopback configuration.~~ at least until a transfer back of a cell without errors is completed within a cell transfer period.

23. (Previously Presented) The system of claim 22, further comprising a central clock generator wherein the start of cell signal generator, the offset controller, and the configuration controller are coupled to the central clock generator.

24. (Currently Amended) The system of claim 22 wherein the ~~sending~~ port ~~controller comprises~~ controllers comprise a serializer configured to serialize cells to be sent and a de-serializer configured to de-serialize received cells.

25. (Previously Presented) The system of claim 22 wherein the cross-connection matrix comprise a N × N crossbar matrix configured to selectively connect N cell input ports with N cell output ports.

26. (Previously Presented) The system of claim 22 wherein the matrix is configured as a unit matrix in the loopback configuration and is configured as a null matrix in the no-transmission configuration.

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27. (Previously Presented) The system of claim 22 wherein the error detector comprises a bit error indicator.

28. (New) A method of configuring a system having a plurality of port controllers coupled to a cross-connection switch, the method comprising:

oscillating the cross-connection switch between loopback transmission periods in which data received by the cross-connection switch is transferred back to a sending port controller and no-transmission periods in which data received by the cross-connection switch is not transferred back to the sending port controller; and

determining, independently for each port controller in the plurality of port controllers, respective cell transmission time offsets by:

sending cells from a respective port controller in the plurality of port controllers to the cross-connection switch;

shifting a start time for cell transmittion by the respective port controller until a complete cell is received by the respective port controller during a loopback transmission period; and

setting the cell transmission time offset for the respective port controller based on the shifted start time for the respective port controller.

29. (New) The method of claim 28, further comprising generating a central clock signal and providing the central clock signal to the plurality of port controllers and the cross-connection switch.